

REMARKS

In the Office Action, the Examiner rejected claims 8-12. The Examiner also objected to the drawings. By the present Response, Applicant has amended claims 8-12 and added claims 14-19. The amendments and new claims do not add any new matter. Upon entry of these amendments, claims 8-12 and 14-19 will be pending in the present application and are believed to be in condition for allowance. In view of the foregoing amendments and the following remarks, Applicant respectfully requests reconsideration and allowance of all pending claims.

Objection to the Drawings

In the Office Action, the Examiner objected to the drawings under 37 CFR 1.83(a). Specifically, the Examiner stated that “[t]he drawings must show every feature of the invention specified in the claims. Therefore, the interposer bond pads lying outside a perimeter of the first semiconductor device must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.” Office Action, page 2. To clarify the claimed subject matter, Applicant has amended claim 8 to remove the feature “both lying outside a perimeter of the first semiconductor device.” For at least these reasons, Applicant respectfully requests withdrawal of the objection to the drawings under 37 CFR 1.83(a).

Claim Rejections Under 35 U.S.C. § 112, First Paragraph

In the Office Action, the Examiner rejected claims 8-12 under 35 U.S.C. § 112, First Paragraph as failing to comply with the written description requirement. Although Applicant does not necessarily agree with the Examiner, Applicant has amended the claims to add clarification, correct typographical errors, and correct any perceived problems with the written description requirement.

Specifically, the Examiner stated that:

[c]laims 8-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application

was filed, had possession of the claimed invention. The newly incorporated limitations in claim 8 require at least a portion of the conductive trace to lie directly underneath and insulated from the second semiconductor device. There is no support in the specification and drawings for these limitations. The drawings in figures 2 and 4 show the traces spaced from the second semiconductor 208 and not directly underneath as currently claimed and there is no support in the specification indicating placement of the trace directly underneath the second semiconductor 208.

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Applicant has amended claim 8 to remove the feature “wherein at least a portion of said conductive trace lies directly underneath and insulated from said second semiconductor device.” Therefore, Applicant respectfully submits that the amended claim 8 resolves any problem with the written description requirement and requests withdrawal of the rejections under Section 112, First Paragraph.

Claim Rejections Under 35 U.S.C. § 112, Second Paragraph

In the Office Action, the Examiner rejected claims 8-12 under 35 U.S.C. § 112, Second Paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Although Applicant does not necessarily agree with the Examiner, Applicant has amended the claims to add clarification, correct typographical errors, and correct any perceived problems with antecedent basis.

Specifically, the Examiner stated that “[c]laim 8 recites the limitation ‘the semiconductor device’ in line 23. There is insufficient antecedent basis for this limitation in the claim, it is not clear if it is referring back to the first or second semiconductor device.” Office Action, page 4. Applicant has amended claim 8 to remove the recited limitation. Therefore, Applicant respectfully submits that the amended claim 8 resolves any problem with antecedent basis and requests withdrawal of the rejections under Section 112, Second Paragraph.

General Comments

Applicant notes that in a prior office action, the Examiner relied on Chikawa et al. (U.S. Publication No. 2001/0020735, hereinafter “Chikawa”) to reject claim 8. Because Applicant has amended claim 8 to remove certain features added in a prior office action and added independent claims 14 and 17, Applicant will also discuss the differences between the claims and Chikawa.

Specifically, claim 8 is directed toward a die package that decreases the length of wires extending between layers of a stacked-die, decreases interlacing, and decreases the pitch of the wires. *See* Specification, para. 5. The die package includes the following layers: a semiconductor device, an interposer, a semiconductor device, and a package substrate. *Id.* at para 15. The interposer includes a pattern of conductive traces to enable two or more wires to be electrically coupled together with the trace within or on the surface of the interposer. *Id.* at para 17. By coupling together two different wires on a single trace, wires can use the interposer as a midway point, such as for connecting a wire between the two semiconductor devices. *Id.* Thus, two short wires may be used rather than one long wire. *Id.*

In contrast, Chikawa is directed toward a re-wiring layer of an IC chip. Chikawa, abstract. The IC chip includes semiconductor chips that are laminated and packaged. *Id.* at para. 1. Wires are used to connect layers together and to connect pads of the re-wiring layer together. *Id.* at para. 33; *see also* FIGS. 2-3; para. 36. The wires are used to connect any of the layers together. *See* FIGS. 2-3. Furthermore, the wires are covered with a passivation film. *Id.* at para. 33.

Applicant notes that independent claim 8 and presently added independent claims 14 and 17 include features that are not found in Chikawa. For example, claim 8, as amended, recites that “the first and second interposer bond pads are formed by a conductive trace.” Furthermore, claim 14 recites “the interposer layer having a first bond pad and a second bond pad formed by a conductive trace extending at least partly within the interposer layer.” These features are not disclosed in Chikawa. In particular, Chikawa teaches using wires to connect bond pads, rather

than using imbedded conductive traces. In addition, claim 17 recites that “each of the plurality of bond wires is coupled between a bond pad of one layer and a bond pad of an adjacent layer.” In contrast, Chikawa appears to teach that wires are coupled across multiple layers of an IC chip as illustrated in FIGS. 2 and 3. Therefore, Applicant stresses that Chikawa does not disclose at least these features found in independent claims 8, 14, and 17.

New Claims

As noted above, Applicant hereby adds new claims 14-19. These claims do not add any new matter. Furthermore, these claims recite features clearly missing from all discussed references. As a result, Applicants respectfully request consideration and allowance of these new claims 14-19.

Conclusion

In view of the remarks set forth above, Applicant respectfully requests reconsideration of the Examiner’s rejections and allowance of all pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicant hereby provides a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor. Furthermore, Applicant authorizes the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 06-1315; Order No. MICS:0213 (FLE/MAN/BAR).

Respectfully submitted,

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